Preliminary Data Sheet

AT&T Microelectronics

ATT7C164
ATT7C165
ATT7C166

High-Speed CMOS SRAM
64 Kbits (16K x 4)
Common I/O

Features

- 16K by 4-bit static RAM with common I/O
- Automatic powerdown during long cycles
- Advanced CMOS technology
- High speed — to 10 ns
- Low-power operation
  — Active: 500 mW typical at 25 ns
  — Standby: 500 µW typical
- Data retention at 2 V for battery backup operation
- Plug-compatible with IDT7188/7198 and CY7C164/166
- Package styles available:
  — 22-/24-pin, plastic DIP
  — 24-pin, plastic SOJ (J-lead)

Description

The ATT7C164, ATT7C165, and ATT7C166 devices are high-performance, low-power, CMOS static RAMs organized as 16,384 words by 4 bits per word. The data-in and data-out signals share I/O pins. The ATT7C164 device has a single active-low chip enable, while the ATT7C165 has two chip enables and a separate output enable. The ATT7C166 Static RAM has a single chip enable and an output enable. Parts are available in four speeds with worst-case access times from 10 ns to 20 ns.

Inputs and outputs are TTL compatible. Operation is from a single 5 V power supply. Power consumption is 500 mW (typical) at 25 ns. Dissipation drops to 75 mW (typical) when the memory is deselected (enable is high).

Two standby modes are available. Automatic powerdown during long cycles reduces power consumption when the memory is deselected or during read or write accesses that are longer than the minimum access time. In addition, data can be retained in inactive storage with a supply voltage as low as 2 V. The ATT7C164, ATT7C165, and ATT7C166 devices consume only 30 µW at 3 V (typical), thereby allowing effective battery backup operation.

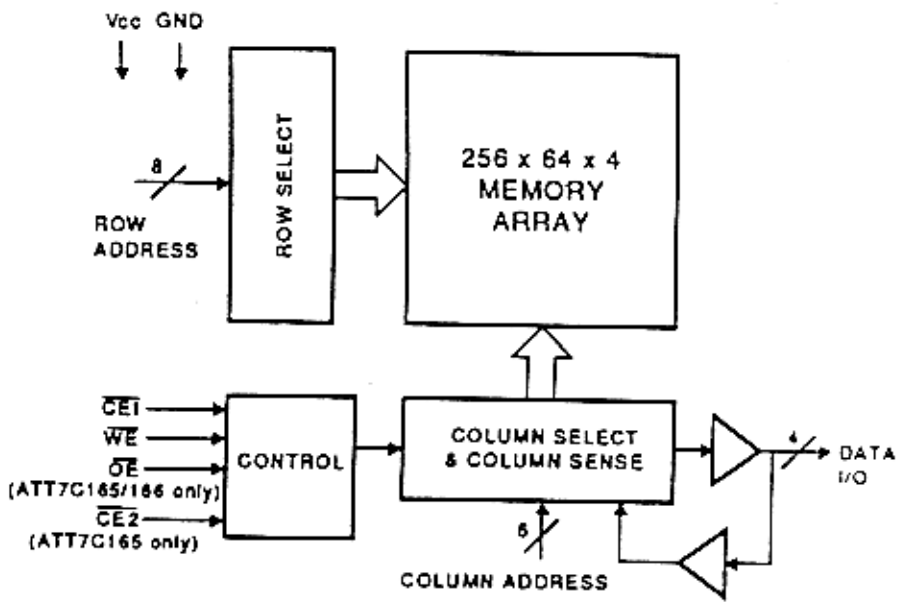


Figure 1. Block Diagram

May 1991

Pin Information

Table 1. ATT7C164 DIP Pin Descriptions

Pin	Name/Function
A0—A13	Address
I/O0—I/O3	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
GND	Ground
Vcc	Power

Table 2. ATT7C164 SOJ Pin Descriptions

Pin	Function
A0—A13	Address
I/O0—I/O3	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
GND	Ground
Vcc	Power
NC	No Connect

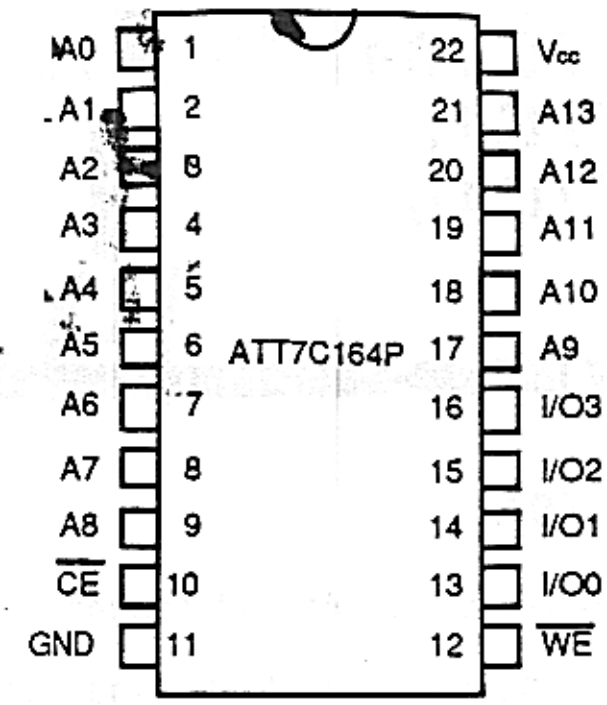


Figure 2. Pin Diagram

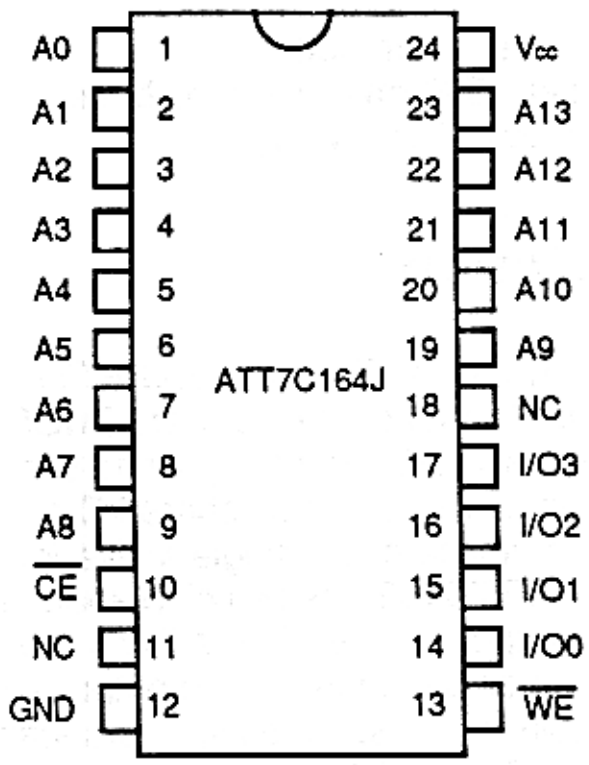


Figure 3. Pin Diagram

Pin Information (continued)

Table 3. ATT7C165 Pin Descriptions

Pin	Name/Function
A0—A13	Address
I/O0—I/O3	Data Input/Output
$\overline{CE1}$ and $\overline{CE2}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
Vcc	Power

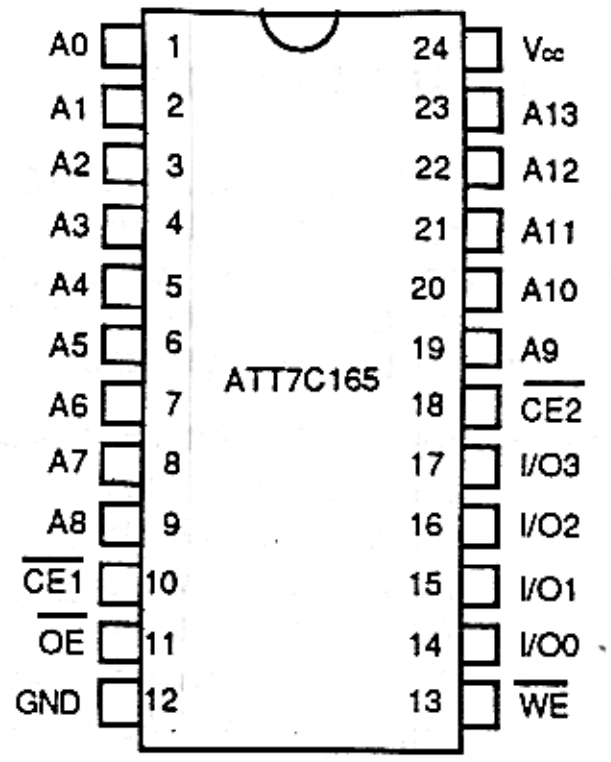


Figure 4. Pin Diagram

Table 4. ATT7C166 Pin Descriptions

Pin	Name/Function
A0—A13	Address
I/O0—I/O3	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
Vcc	Power
NC	No Connect

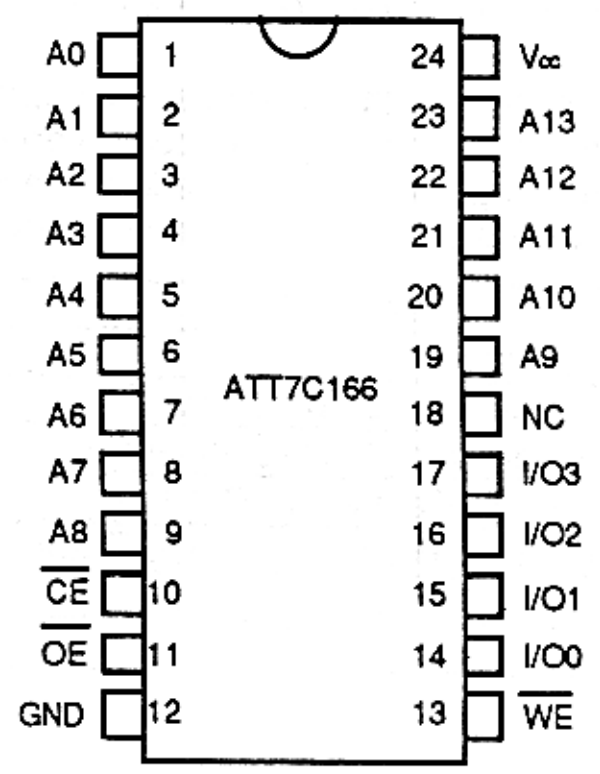


Figure 5. Pin Diagram

Functional Description

The ATT7C164, ATT7C165, and ATT7C166 devices provide asynchronous (unclocked) operation with matching access and cycle times. An active-low chip enable and a 3-state I/O bus simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A0 through A13. For the ATT7C164, reading from a designated location is accomplished by presenting an address and then taking $\overline{CE}$ low while $\overline{WE}$ remains high. For the ATT7C166 device, both $\overline{CE1}$ and $\overline{OE}$ must be low. The ATT7C165 device requires $\overline{CE1}$, $\overline{CE2}$, and $\overline{OE}$ to be low. The data in the addressed memory location then appears on the data-out pin within one access time. When $\overline{CE}$ or $\overline{OE}$ is high or $\overline{WE}$ is low, the output pin stays in a high-impedance state.

Writing to an addressed location is accomplished when the $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal can be used to terminate the write operation. Data-in and data-out signals have the same polarity.

Latch-up and static discharge protection are provided on-chip. The ATT7C164, ATT7C165, and ATT7C166 devices can withstand an injection of up to 200 mA on any pin without damage.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	−65	150	°C
Operating Ambient Temperature	T_A	−55	125	°C
Supply Voltage with Respect to Ground	Vcc	−0.5	7.0	V
Input Signal with Respect to Ground	—	−3.0	7.0	V
Signal Applied to High-impedance Output	—	−3.0	7.0	V
Output Current into Low Outputs	—	—	25	mA
Latch-up Current	—	>200	—	mA

Recommended Operating Conditions

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation	0 °C to 70 °C	4.5 V ≤ Vcc ≤ 5.5 V
Data Retention	0 °C to 70 °C	2.0 V ≤ Vcc ≤ 5.5 V

Electrical Characteristics

Over all Recommended Operating Conditions

Table 5. General Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage:						
High	V_{OH}	I_{OH} = –4.0 mA, Vcc = 4.5 V	2.4	—	—	V
Low	V_{OL}	I_{OL} = 8.0 mA	—	—	0.4	V
Input Voltage:						
High	V_{IH}	—	2.2	—	Vcc + 0.3	V
Low[1]	V_{IL}	—	–3.0	—	0.8	V
Input Current	I_{IX}	Ground ≤ V_I ≤ Vcc	–10	—	10	µA
Output Leakage Current	I_{OZ}	Ground ≤ Vo ≤ Vcc, $\overline{CE}$ = Vcc	–10	—	10	µA
Output Short Current	I_{OS}	Vo = Ground, Vcc = Max[2]	—	—	–350	mA
Vcc Current:						
Inactive[3]	I_{CC2}	—	—	15	30	mA
Standby[4]	I_{CC3}	—	—	100	500	µA
DR Mode	I_{CC4}	Vcc = 2.0 V[5]	—	10	250	µA
Capacitance:						
Input (Except $\overline{CE2}$ /165)	C_I	T_A = 25 °C,	—	—	7	pF
Input ($\overline{CE2}$ /165)	C_I	Vcc = 5.0 V	—	—	10	pF
Output	Co	Test frequency = 1 MHz[6]	—	—	7	pF

1. This device provides hard clamping of transient undershoot. Input levels below ground are clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond-wire fusing constraints.
2. Duration of the output short-circuit should not exceed 30 s.
3. Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165) ≥ V_{IH}.
4. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165) = Vcc. Input levels are within 0.5 V of Vcc or ground.
5. Data retention operation requires that Vcc never drops below 2.0 V. $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165) must be ≥ Vcc – 0.3 V. For all other inputs, V_{IN} ≥ Vcc – 0.3 V or V_{IN} < 0.3 V is required to ensure full powerdown.
6. This parameter is not 100% tested.

Table 6. Electrical Characteristics by Speed

Parameter	Symbol	Test Condition	Speed (ns)					Unit
			25	20	15	12	10	
Vcc Current, Active	I_{CC1}	*	100	125	160	190	205	mA

* Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165) and $\overline{WE}$ ≤ V_{IL}. Input pulses are 0 V to 3.0 V.

Timing Characteristics

Table 7. Read Cycle[1, 2, 3, 4]

Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 12), and output loading for specified I_{OL} and I_{OH} +30 pF (see Figure 11A).

Symbol	Parameter	Speed									
		25		20		15		12		10	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tADXADX, tCELCEH	Read-cycle Time	25	—	20	—	15	—	12	—	10	—
tADXDOV	Address Change to Output Valid[5, 6]	—	25	—	20	—	15	—	12	—	10
tADXDOX	Address Change to Output Change	3	—	3	—	3	—	3	—	3	—
tCELDOV	Chip Enable Low to Output Valid[5, 7]	—	25	—	20	—	15	—	12	—	10
tCELDOZ	Chip Enable Low to Output Low-Z[8, 9]	3	—	3	—	3	—	3	—	3	—
tCEHDOZ	Chip Enable High to Output High-Z[8, 9]	—	10	—	8	—	8	—	5	—	4
tOELDOV	Output Enable Low to Output Valid	—	12	—	10	—	8	—	6	—	4
tOELDOZ	Output Enable Low to Output Low-Z[8, 9]	0	—	0	—	0	—	0	—	0	—
tOEHDOZ	Output Enable High to Output High-Z[8, 9]	—	10	—	8	—	5	—	5	—	4
tCELICH, tADXICH	Chip Enable Low or Address Change to Powerup[10, 11]	0	—	0	—	0	—	0	—	0	—
tICHICL	Powerup to Powerdown[10, 11]	—	25	—	20	—	20	—	20	—	18

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADXWEH (Table 8) is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
2. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 11B. This parameter is sampled and not 100% tested.
3. All address timings are referenced from the last valid address line to the first transitioning address line.
4. $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the AT7C165) or $\overline{WE}$ must be high during address transitions.
5. This product is a very high-speed device, and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground.. To avoid signal reflections, proper terminations must be used.
6. $\overline{WE}$ is high for the read cycle.
7. The chip is continuously selected ($\overline{CE}$ low; $\overline{CE1}$ and $\overline{CE2}$ low).
8. All address lines are valid prior to or coincident with the $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165) transition to low.
9. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
10. This parameter is not 100% tested.
11. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165); (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active; $\overline{CE1}$ and $\overline{CE2}$ active on the ATT7C165); (3) transition on any address line ($\overline{CE}$ active; $\overline{CE1}$ and $\overline{CE2}$ active on the ATT7C165); or (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active; $\overline{CE1}$, $\overline{CE2}$, and $\overline{WE}$ active on the ATT7C165). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Timing Characteristics (continued)

Table 8. Write Cycle[1, 2, 3, 4] (See Figures 8, 9, and 10.)

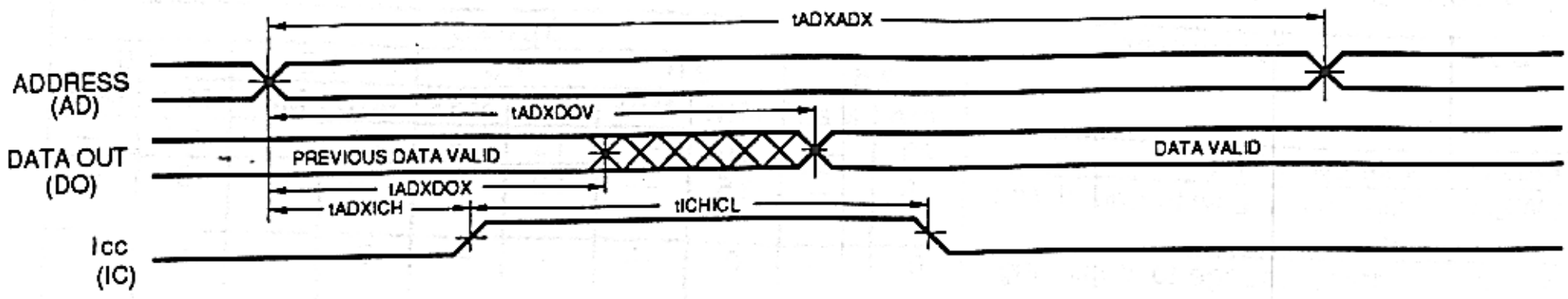
Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 12), and output loading for specified I_{OL} and I_{OH} +30 pF (see Figure 11A).

Symbol	Parameter	Speed									
		25		20		15		12		10	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tADXADX	Write-cycle Time	20	—	20	—	15	—	12	—	10	—
tCELWEH	Chip Enable Low to End of Write Cycle	15	—	15	—	12	—	10	—	8	—
tADXWEX, tADXWEL	Address Change to Beginning of Write Cycle	0	—	0	—	0	—	0	—	0	—
tADXWEH	Address Change to End of Write Cycle	15	—	15	—	12	—	10	—	8	—
tWEHADX	End of Write Cycle to Address Change	0	—	0	—	0	—	0	—	0	—
tWELWEH	Write Enable Low to End of Write Cycle	15	—	15	—	12	—	10	—	8	—
tDIZWEH, tDIXCEH	Data Valid to End of Write Cycle	10	—	10	—	7	—	6	—	5	—
tWEHDIV, tWEHDIX	End of Write Cycle to Data Change	0	—	0	—	0	—	0	—	0	—
tWEHDOZ	Write Enable High to Output Low-Z[5, 6]	0	—	0	—	0	—	0	—	0	
tWELDOZ	Write Enable Low to Output High-Z[5, 6]	—	7	—	7	—	5	—	4	—	4
tCELICH	Chip Enable Low to Powerup[7, 8]	0	—	0	—	0	—	0	—	0	—
tWELICH	Write Enable Low to Powerup[7, 8]	0	—	0	—	0	—	0	—	0	—
tCEHVCL	Chip Enable High to Data Retention[7]	0	—	0	—	0	—	0	—	0	—

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADXWEH is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
2. All address timings are referenced from the last valid address line to the first transitioning address line.
3. $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165) or $\overline{WE}$ must be high during address transitions.
4. This product is a very high-speed device, and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.
5. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
6. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 11B. This parameter is sampled and not 100% tested.
7. This parameter is not 100% tested.
8. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165); (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active; $\overline{CE1}$ and $\overline{CE2}$ active on the ATT7C165); (3) transition on any address line ($\overline{CE}$ active; $\overline{CE1}$ and $\overline{CE2}$ active on the ATT7C165); or (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active; $\overline{CE1}$, $\overline{CE2}$, and $\overline{WE}$ active on the ATT7C165). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Timing Characteristics (continued)

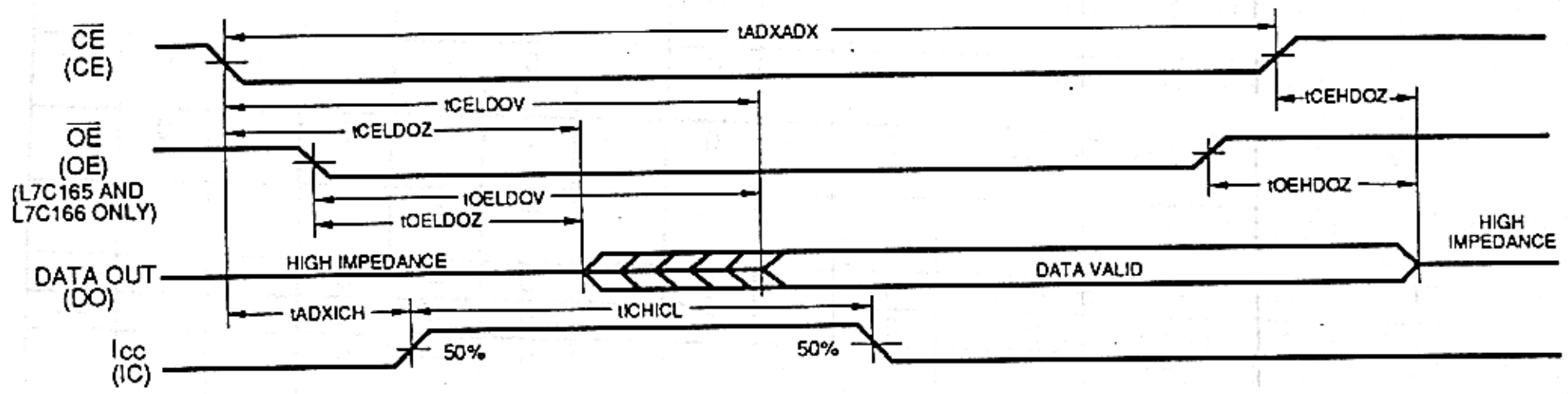
Timing Diagrams



Notes:
$\overline{WE}$ is high for the read cycle.

The chip is continuously selected ($\overline{CE}$ low on the ATT7C164 and 166; $\overline{CE1}$ and $\overline{CE2}$ low on the ATT7C165).

Figure 6. Read Cycle — Address-Controlled

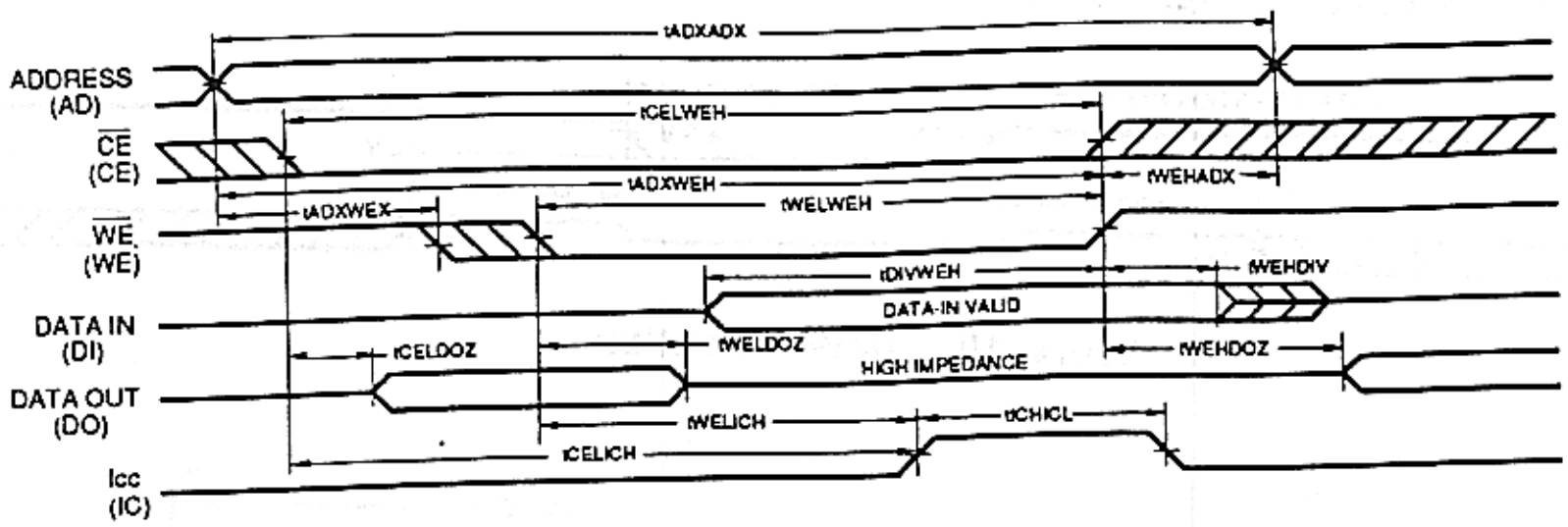


Notes:
$\overline{WE}$ is high for the read cycle.

All address lines are valid prior to or coincident with the $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165) transition to low .

Figure 7. Read Cycle — $\overline{CE}$ / $\overline{OE}$ -Controlled

Timing Characteristics (continued)



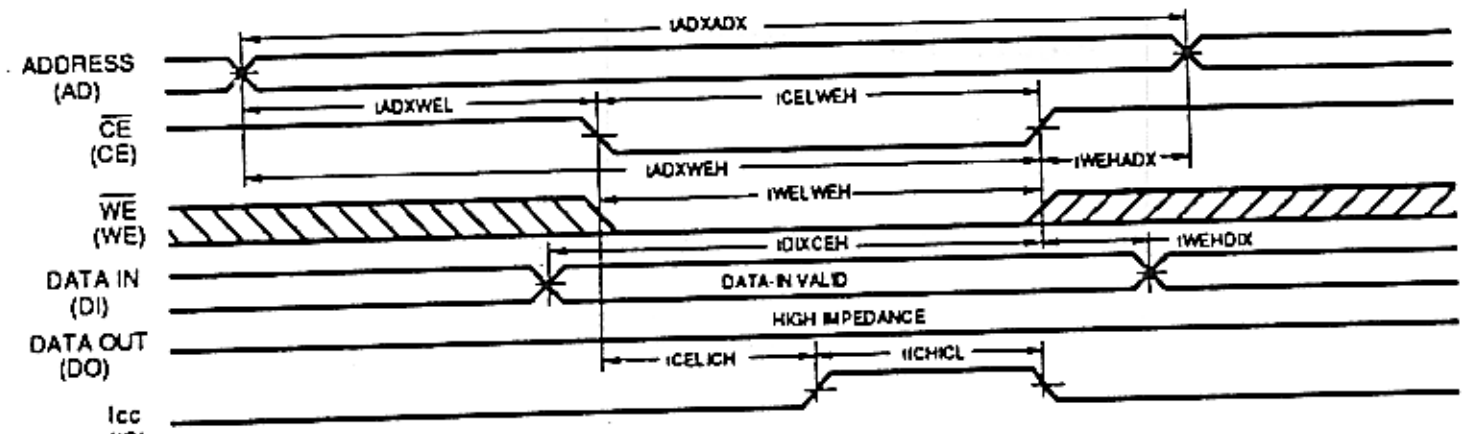
Notes:
The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165) low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referred to the signal that falls last or rises first.

If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165) going low, the output remains in a high-impedance state.

If $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165) goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165); (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active; $\overline{CE1}$ and $\overline{CE2}$ active on the ATT7C165); (3) transition on any address line ($\overline{CE}$ active; $\overline{CE1}$ and $\overline{CE2}$ active on the ATT7C165); or (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active; $\overline{CE1}$, $\overline{CE2}$, and $\overline{WE}$ active on the ATT7C165). The device automatically powers down from I_{CC1} to I_{CC2} after t_{ICHICL} has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Figure 8. Write Cycle — $\overline{WE}$-Controlled



Notes:
The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165) low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referred to the signal that falls last or rises first.

If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165) going low, the output remains in a high-impedance state.

If $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165) goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$ ($\overline{CE1}$ and $\overline{CE2}$ on the ATT7C165); (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active; $\overline{CE1}$ and $\overline{CE2}$ active on the ATT7C165); or (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active; $\overline{CE1}$, $\overline{CE2}$, and $\overline{WE}$ active on the ATT7C165). The device automatically powers down from I_{CC1} to I_{CC2} after t_{ICHICL} has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Figure 9. Write Cycle — $\overline{CE}$-Controlled

Timing Characteristics (continued)

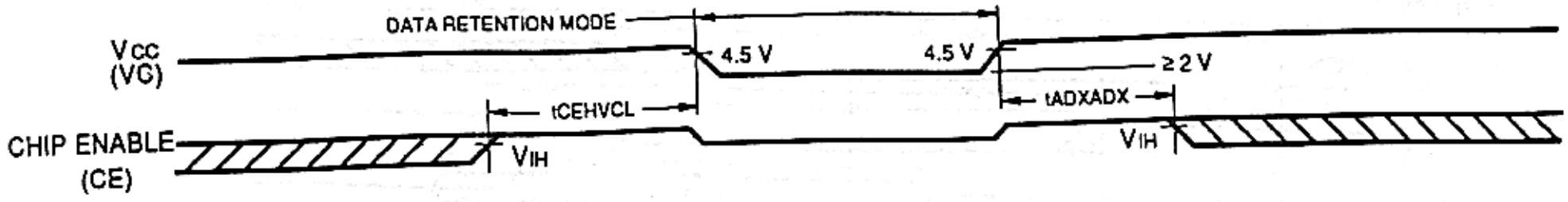
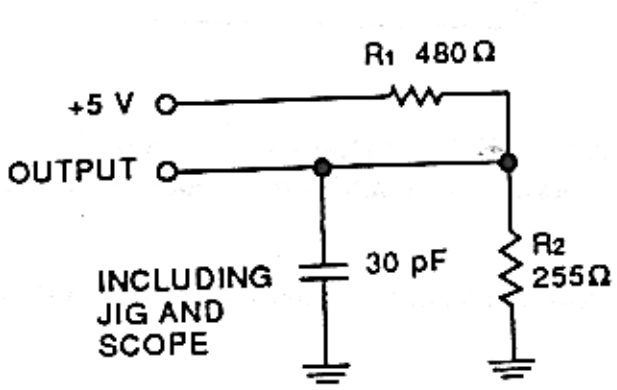
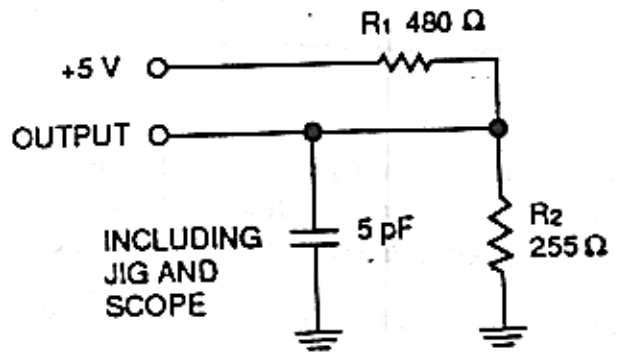


Figure 10. Data Retention



A.



B.

Figure 11. Test Loads

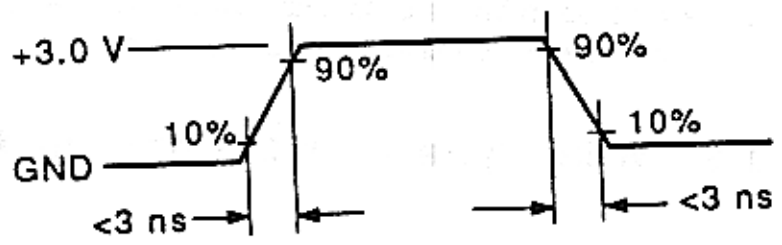
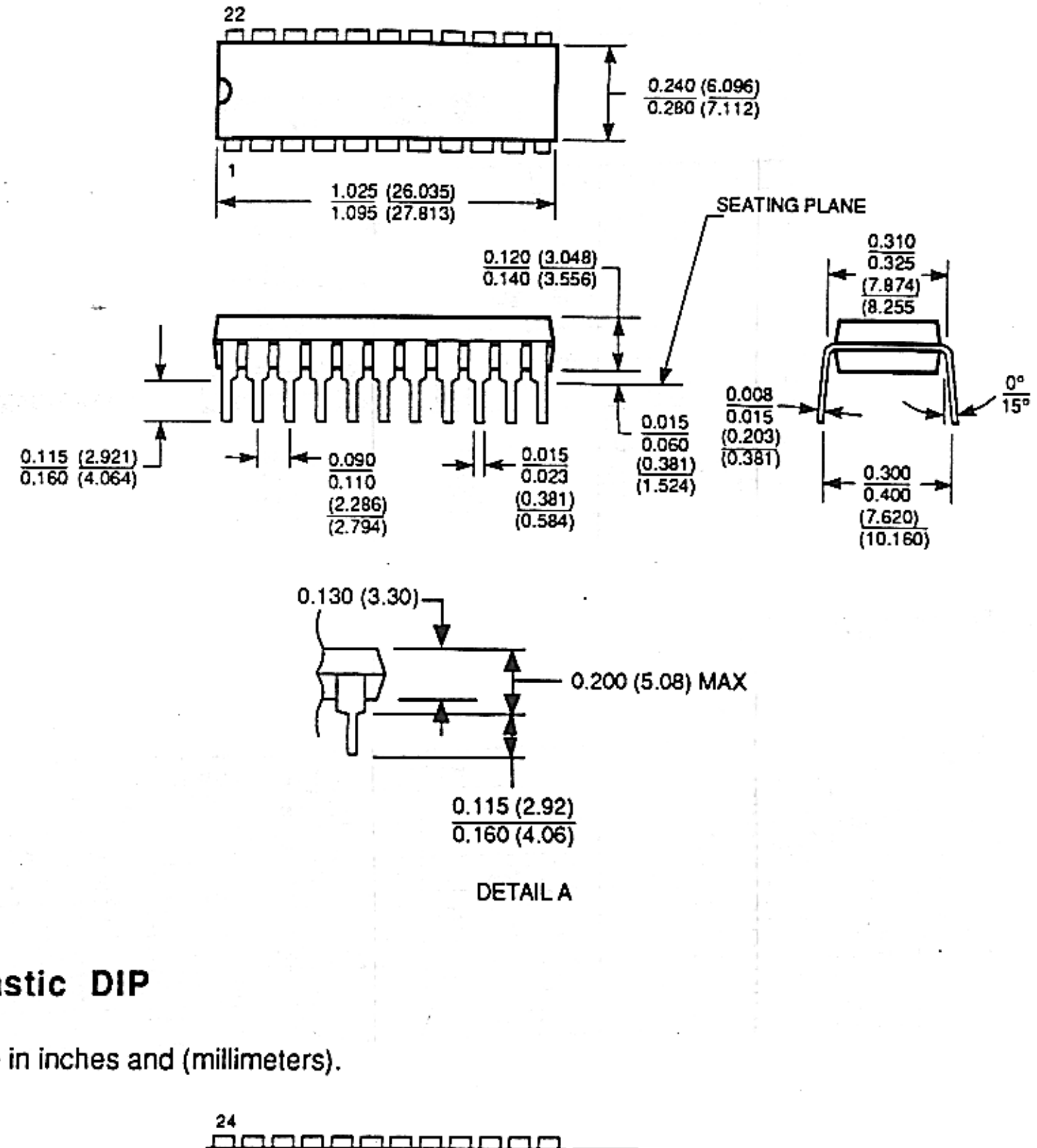


Figure 12. Transition Times

Outline Diagrams

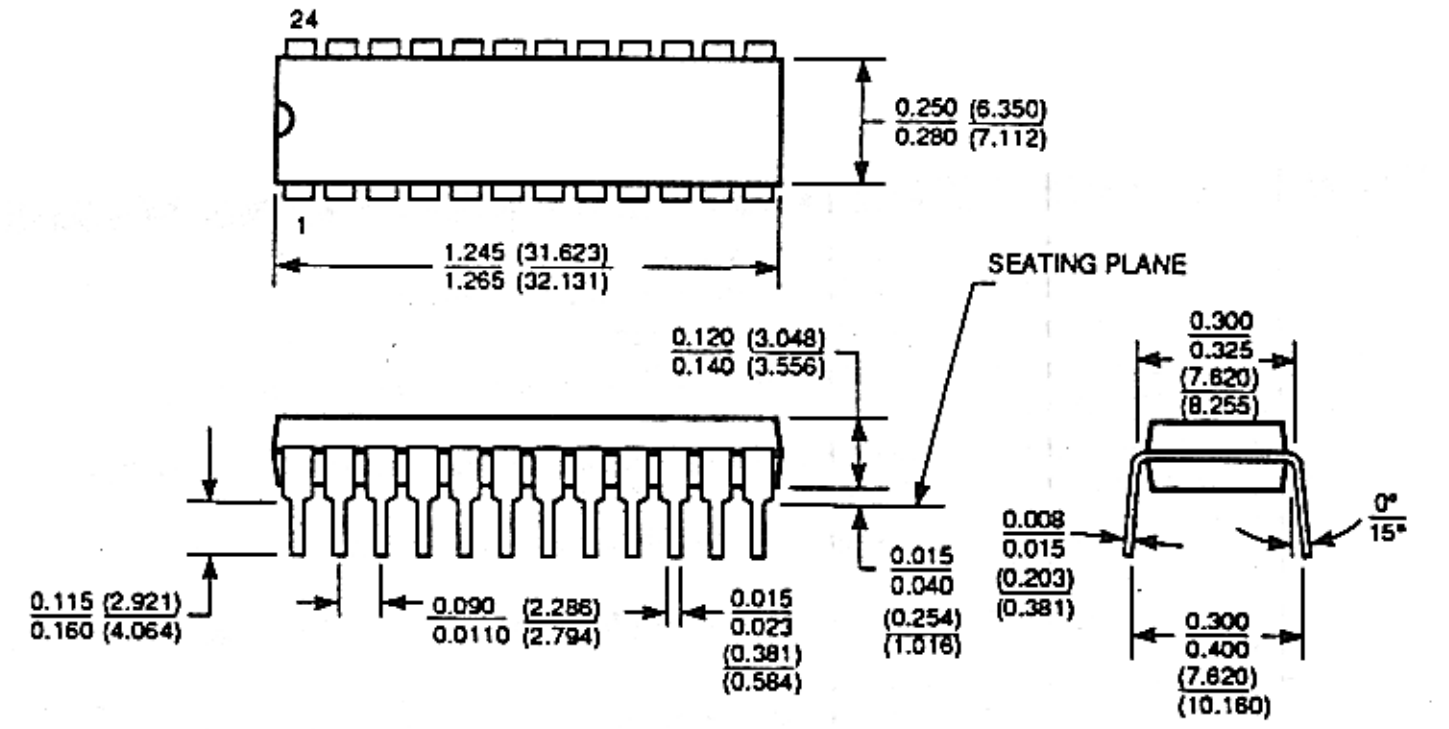
22-Pin, Plastic DIP

Dimensions are in inches and (millimeters). This device may be provided with half-end leads or full-end leads (Detail A) at AT&T's discretion.



24-Pin, Plastic DIP

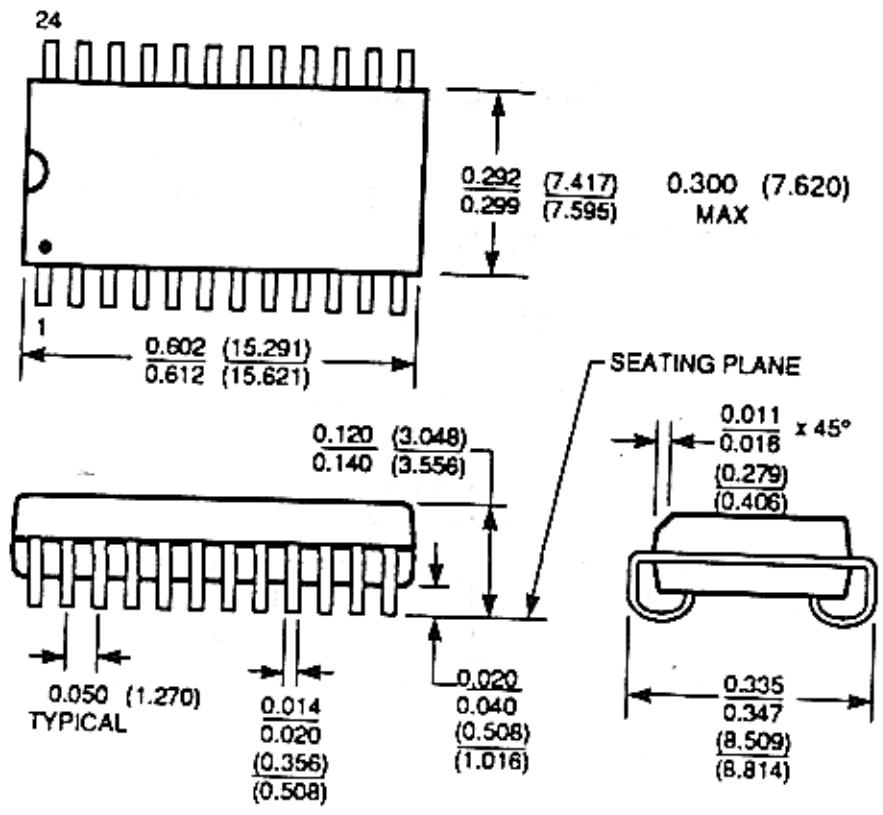
Dimensions are in inches and (millimeters).



Outline Diagrams (continued)

24-Pin, Plastic SOJ

Dimensions are in inches and (millimeters).



Ordering Information

Operating Range 0 °C to 70 °C on all devices.

Device #	Package Style	Performance Speed				
		25 ns	20 ns	15 ns	12 ns	10 ns
ATT7C164	22-Pin, Plastic DIP	ATT7C164P–25	ATT7C164P–20	ATT7C164P–15	ATT7C164P–12	ATT7C164P–10
	24-Pin, Plastic SOJ	ATT7C164J–25	ATT7C164J–20	ATT7C164J–15	ATT7C164J–12	ATT7C164J–10
ATT7C165	24-Pin, Plastic DIP	ATT7C165P–25	ATT7C165P–20	ATT7C165P–15	ATT7C165P–12	ATT7C165P–10
	24-Pin, Plastic SOJ	ATT7C165J–25	ATT7C165J–20	ATT7C165J–15	ATT7C165J–12	ATT7C165J–10
ATT7C166	24-Pin, Plastic DIP	ATT7C166P–25	ATT7C166P–20	ATT7C166P–15	ATT7C166P–12	ATT7C166P–10
	24-Pin, Plastic SOJ	ATT7C166J–25	ATT7C166J–20	ATT7C166J–15	ATT7C166J–12	ATT7C166J–10